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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.

EXAMINER	
ART UNIT	PAPER NUMBER
	13

DATE MAILED:

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary

Application No.	Applicant(s)
09/045,041	Fujisawa
Examiner	**Group Art Unit**
Hugh Jones	2123

☒ Responsive to communication(s) filed on *Dec 21, 2000*

☐ This action is **FINAL.**

☐ Since this application is in condition for allowance except for formal matters, **prosecution as to the merits is closed** in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

A shortened statutory period for response to this action is set to expire *3* month(s), or thirty days, whichever is longer, from the mailing date of this communication. Failure to respond within the period for response will cause the application to become abandoned. (35 U.S.C. § 133). Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

Disposition of Claim

☒ Claim(s) *9-45* is/are pending in the applicat

Of the above, claim(s) _____ is/are withdrawn from consideration

☐ Claim(s) _____ is/are allowed.

☒ Claim(s) *9-45* is/are rejected.

☐ Claim(s) _____ is/are objected to.

☐ Claims _____ are subject to restriction or election requirement.

Application Papers

☐ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.

☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

☒ The proposed drawing correction, filed on *Dec 21, 2000* is ☒ approved ☐ disapproved.

☐ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

☒ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

☒ All ☐ Some* ☒ None of the CERTIFIED copies of the priority documents have been

☒ received.

☐ received in Application No. (Series Code/Serial Number) _____ .

☐ received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

*Certified copies not received: _____

☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

☒ Notice of References Cited, PTO-892

☐ Information Disclosure Statement(s), PTO-1449, Paper No(s). _____

☐ Interview Summary, PTO-413

☐ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Notice of Informal Patent Application, PTO-152

— SEE OFFICE ACTION ON THE FOLLOWING PAGES —

DETAILED ACTION

Claim Rejections - 35 USC § 101

1. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

2. **Claims 9-45 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.** The limitations of claims 9-20 and 45 are directed to abstract ideas. There is no pre-processing or post-processing of real world data. The limitations of claims 21-32 and 33-44 are directed to *systems and apparatus, respectively, incorporating* algorithmic programs on a computer. However, a claim directed at execution requires further consideration. The mere fact that a hardware element is recited in a claim does not necessarily limit the claim to a specific machine. *Cf.* In re *Iwahashi*, 888 F.2d 1370, 1374-75, 12 USPQ2d 1908, 1911-12 (Fed. Cir. 1989), *cited with approval in Alappat*, 33 F.3d at 1544 n.24, 31 USPQ2d at 1558 n.24. If a product claim encompasses *any* and every computer implementation of a process, when read in light of the specification, it should be examined on the basis of the underlying process. Such a claim is recognized as such because it will:

- define the physical characteristics of the computer component exclusively as functions or steps to be performed on or by a computer, and
- encompass *any and every* product in the stated class (e.g., computer, computer-readable memory) *configured in any manner* to perform that process.

Thus, even if the program were being executed, but there was no pre-processing or post-processing of real world data, i.e., *the underlying process was non-statutory*, the claims would not be statutory. Applicant is attempting to claim a simulation without any connection to real world data.

3. Claims 9-45 are rejected under 35 U.S.C. 101 because the claimed invention is not supported by either a specific asserted utility or a well established utility.

4. Claims 9-45 also rejected under 35 U.S.C. 112, first paragraph. Specifically, since the claimed invention is not supported by either a asserted utility or a well established utility for the reasons set forth above, one skilled in the art clearly would not know how to use the claimed invention.

Claim Rejections - 35 USC § 112

5. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

6. Claims 9-45 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. *The claims are exteremely difficult to interpret. For illustrative purposes, claims 9-20 are considered to exemplify all claims, as per these issues. Examples are provided for Representative - Representative is responsible for correcting all other or similar instances.*

7. The issue has to do with *compressing* and *integrating*. Examiner interprets Representative's remarks on pages 10-11 of paper # 7 to mean that equivalent partial circuits are combined or merged in some fashion. It it not clear how they are *combined* and if the *combining* itself causes problems. For example, how could two partial circuits, which presumably could be seperated by other circuits, be combined or merged without affecting the actual as well as simulted behavior? Would the new entity create structural, functional and logical inconsistencies or problems when it is, presumably, integrated with the rest of the circuit?

8. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

9. *The claims are exteremely difficult to interpret. For illustrative purposes, claims 9-20 are considered to exemplify all claims, as per these issues. Examples are provided for Representative - Representative is responsible for correcting all other or similar instances.*

10. Claims 9-45 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Note the following *examples*:

- claim 1: *extracting* how?
- claim 1: what *circuit*?
- claim 1: *inspect* how?
- claim 1: are the partial circuits related in any way (such as proximity, or does it matter)?

- claim 1: what *is configurations*? Does this mean physical and structural?

- claim 1: *exhibiting* how? How is this determined?

- claim 1: what is *equivalent operational characteristcs*?

- claim 1: what is *equivalent operational characteristcs based on the configurations*? What is the connection between the two (what does *based* mean?).

- claim 1: *compressed* how?

- claim 1: what kind of simulation?

- claim 1: what is meant by *integrating* and how is it carried out? Is this the same as merging equivalent circuit blocks (as in class/sub-class 716/3)?

- claim 1: Is the simulation carried out *after integration* or *after compression* by integrating (issue of grammar).

- claim 10: what is *connectional relationships*? This does not provide the reader with useful information.

- claim 11: what is *inspecting is based on the corresponding component elements*? This does not provide the reader with useful information.

- claim 13: what is meant by *mutually consistent*?

- claim 14: what is meant by *mutually inconsistent*?

- claims 16-17: what is *intensity* and *intensity of the influence*?

- claim 18: *frequency of shifting* of what?

11. Claims 9-49 are rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential steps, such omission amounting to a gap between the steps. See MPEP § 2172.01. The omitted steps are:

- claim 1: where is the *compressing* step?

- claim 1: what is *equivalent operational characteristcs based on the configurations*? *Based* seems to imply a step.

- claim 1: how is the *compression* carried out? There appears to be a step missing which is related to *based.*

- claim 1: how is the *integration* carried out? There appears to be a step missing which is related to *based.*

- claim 10: what is *inspecting is based on the connectional relationships*? This does not provide the reader with useful information. There appears to be a step missing which is related to *based.*

- claim 11: what is *inspecting is based on the corresponding component elements*? This does not provide the reader with useful information. There appears to be a step missing which is related to *based.*

- claims 13-14: *judging* how?

- claim 15: *assessing* how?

- claim 15: *tracing* how?

- claim 16: *based* on the intensity - based how?

12. Claim 15 is rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential structural cooperative relationships of elements, such omission amounting to a gap between the necessary structural connections. See MPEP § 2172.01. The omitted structural cooperative relationships are: there is no description of the *linking*.

Claim Rejections - 35 USC § 102

13. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

14. Claims 9-45 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Filseth.

Filseth discloses (abstract):

> *"The invention describes a method for expanding (flattening) hierarchical descriptions of electronic circuits into flat descriptions. The method is characterized by two processes: one which eliminates feed-through and implicit signals, and another which pre-plans the layout of the flattened data structure before flattening. The flattening process may then take advantage of a number of resulting efficiencies to operate more quickly than present flatteners."*

Col. 1, line 12 to col. 2, line 15 disclose:

> "Modern electronic systems are often designed with the assistance of electronic computer-aided-design tools, hereinafter referred to as ECAD tools. Typically, a user will capture a schematic diagram or other convenient form of circuit description on a display screen of an ECAD system using any of a number of interactive or automatic (e.g., module generators, silicon compilers, logic

synthesizers) techniques widely known in the present art. As a part of the design process, a designer will typically capture and compile a design and then simulate it through the use of a logic simulator.

Complex logic circuits are customarily described hierarchically, but are simulated flat (or fully expanded). This means that if a module A in a user's design contains three instances of a submodule B, and submodule B contains two instances of another submodule C, the user will declare only two copies of submodule C in the process of capturing his design, but because of the implied replication in the user's design, the simulator will simulate six instances of submodule C for each instance of module A, since there are two instances of submodule C in each of the three instances of submodule B comprising module A. When such a circuit description is modified and re-simulated, a program must read the hierarchical description and produce a flat, or fully expanded, description of the hierarchical design before the simulation may be accomplished. A program that accomplishes this function is called a "linker" or "flattener". Hereinafter, the terms "link" and "flatten" will be used interchangeably. All modern ECAD systems include such a program, since a flat circuit description is too cumbersome for users to create directly, and a hierarchical description cannot easily be simulated directly, because the many different instances of the submodules of a hierarchy may be in different states during simulation and must be dealt with individually by the simulator.

Inputs to a linker generally consist of a set of circuit descriptions of different hierarchical levels or "modules" in a circuit. Each module description contains a list of submodules, internal wires (also called "signals" or "nets") , and I/O (input/output) pins. Each I/O pin of the module's submodules is connected to one of the module's internal wires. Some of those wires are in turn connected to I/O pins of the module itself. The details of these interconnections are also a part of the module description. In addition, the module description contains the name of the module, the name of each submodule, internal wire, and I/O pin the module comprises. Any module may itself be a submodule of another module; further illustrating the impact of hierarchy on a design.

These inputs to the linker may be either memory-resident data structures, or data structures contained in files on an on-line mass-storage device. Since it is a relatively trivial process to move data structures between files and memory, it will be assumed hereinafter without loss of generality that all linker inputs are memory-resident.

The output from a linker is a flattened, or expanded, description of the input circuit descriptions. It contains an explicit representation of every copy of every bottom-level submodule in the circuit design. The term "bottom-level submodule" refers to submodules at the bottom level of a circuit hierarchy for which no further expansion is possible, i.e., submodules which comprise no further submodules. Hereinafter, such bottom-level submodules will be referred to interchangeably as "primitives". Each primitive has I/O connections (pins) which are explicitly represented, but which may be replicated in multiple instances of the primitive. Connections between I/O pins of primitives may be made at a higher level of hierarchy where the details of the lower levels of circuit interconnection are not explicitly visible, but which do exist."

See, also: col. 2, line 16 to col. 6, line 55.

Claim Rejections - 35 USC § 103

15. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

16. Claims 9-45 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shinsha et al. *or* Wang et al. *or* Kuehlmann et al..

17. Shinsha et al. discloses (abstract):

> "A logic design automation system examines correspondence relationship among sublogics in intermediate gate-level logic (containing neither physical design information nor manually optimized logic design information) produced from updated functional-level logic and current gate-level logic (containing the above information) to identify corresponding sublogics and non-corresponding sublogics of the gate-level logics with reference to primary input/output signals and input/output gates. For the corresponding sublogics, the corresponding sublogics of the current gate-level logic are selected, and for the non-corresponding sublogics, the non-corresponding sublogics of the intermediate gate-level logic are selected. The selected sublogics are combined to synthesize updated gate-level logic which preserved therein the physical design information and the manually optimized logic design information for portions of the current gate-level logic which need not be modified."

Col. 1, line 49 to col. 2, line 8 disclose:

> "It is the object of the present invention to provide a novel method in a logic design automation system in which physical design information and manually optimized logic design information contained in portions of the current gate-level logic which need not be modified in updating the functional-level logic in the physical design phase are automatically succeeded to the updated gate-level logic.
>
> In accordance with the present invention, in a logic design automation system for automatically synthesizing gate-level logic from functional-level logic, the method comprises the steps of

> synthesizing intermediate gate-level logic containing neither physical design information nor manually optimized logic design information from the updated functional-level logic when portions of the current functional-level logic corresponding to the current gate-level logic containing the above information are modified, identifying corresponding sublogics and non-corresponding sublogics which are common and not common to the current gate-level logic and the intermediate gate-level logic, respectively, and combining the corresponding sublogics of the current gate-level logic with the non-corresponding sublogics of the intermediate gate-level logic to synthesize updated gate-level logic preserving physical design information and manually optimized logic design information for portions of the current gate-level logic which need not be modified."

See, also: fig. 1-2, 6, 17; col. 5.

18. Wang et al. disclose, "*Restructuring binary decision diagrams based on functional equivalence.*" The abstract discloses:

> "A method to restructure binary decision diagrams (BDDs) from a given input ordering to any other ordering is proposed. This technique is based on the concept of functional equivalence and BBDs structure equivalence. A transpositional operator is developed to implement the transformation. It is shown that this transformation is used to find a good input variable ordering for BBDs a good input partition for communication complexity based multilevel logic synthesis. Experimental results are presented.
>
> Index Terms: Boolean functions; equivalence classes; communication complexity; logic design; multivalued logic; restructuring method; Boolean functions; binary decision diagrams; functional equivalence; transpositional operator; input variable ordering; input partition; communication complexity; multilevel logic synthesis"

See, also: page 261 (functional and structural equivalence checking, structure modification); fig. 2 (structural equivalence); page 263 (Equivalence class, transpositional operator and variable ordering of BDD).

19. Kuehlmann et al. discloses, "*Equivalence checking using cuts and heaps.*" See: abstract; col. 1, pahe 263 (structural and functional equivalence); section 3 (merging of equivalent vertices). Also note fig. 2.

20. (Shinsha et al. *or* Wang et al. *or* Kuehlmann et al.) teach all of the limitations, but they do not explicitly teach simulation *before* device fabrication in order to verify functional and behavioral circuit characteristics. It would have been obvious to one of ordinary skill in the art at the time of the invention to carry out such a simulation because this is standard engineering practice - it would be costly and time consuming to fabricate a circuit which did not perform according to design specifications.

New Claim Rejections - 35 USC § 102

21. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

22. Claims 9-45 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Yokomizo et al. or Chakrabarti et al..

23. Yokomizo et al. disclose "*A new circuit recognition and reduction method for pattern based circuit simulation.*" They further disclose a ***novel circuit recognition and reduction method to extract subcircuit data corresponding to the critical paths, including all relevant parasitics and internal loading. Circuit elements extracted from layout pattern data are***

combined to reconstruct logic gates, and a structure of the gates is recognized by the connection between the gate terminals. The recognized circuit data is reduced by tracing signal flows and picking up the gates along the specified critical paths. The circuit elements connected between a remaining net and an eliminated net are terminated as capacitive loads, and parasitic elements are merged or eliminated when the estimated error is permissible, compared with the specified error tolerance. The error is estimated by the first-order moment of the impulse response. Results on logic macrocells and memory peripheral control circuits show that the reduced circuit sizes are 15-50 times smaller, resulting in circuit simulation speedups of 50-300 times faster. See pp. 9.4.2-9.4.3.

24. Chakrabarti et al. disclose "*An improved hierarchical test generation technique for combinational circuits with repetitive sub-circuits.*" They also disclose an ***improved hierarchical testing algorithm for combinational circuits with repetitive sub-circuits using the bus fault model. This model exploits the regularity of a circuit by grouping together identical gate-level sub-circuits into high-level sub-circuits***. Though the existing test generation techniques using this model reduces the required time substantially in many cases, it fails on encountering incompatibility between the inputs and outputs of high-level modules. The algorithm proposed helps in resolving high level incompatibility. The concept of a state transition graph has been used and it has been shown that resolving incompatibility at the high level is equivalent to finding a loop in the state transition graph. ***The technique is hierarchical in the sense that the original modeled high-level circuit is sub-divided into a number of components as soon as an***

incompatibility is encountered. The results of implementation of the algorithm for a class of combinational circuits indicate a significant reduction in the test generation time and complete fault coverage thus validating our technique. See section 4.

25. Claims 9-45 are rejected under 35 U.S.C. 102(e) as being clearly anticipated by Hachiya or Fujisawa.

26. Hachiya discloses a circuit partitioning apparatus comprising an update operation times ounting section that decomposes into the product of triangular matrixes the circuit matrix of each subcircuit composed of clusters generated by an initial clustering section; and a computation time prediction section that uses the results of counting by the update operation times counting section to predict simulation computation time required by a simulation execution time, prior to the execution of simulation, wherein the initial clustering section and a min-cut section feed back the results of the prediction section to carry out clustering and min-cut in order to create subcircuits that require equal computation time for circuit simulation. Note fig. 2 (including a merge operation), fig. 5, fig. 7 (including a merge operation), fig. 8 and fig. 9 (merging of clusters prior to simulation).

27. Fujisawa discloses that paths from a block that includes the node that is the object of analysis to another block are searched for by a path search section for all blocks in a circuit; and a ***depth judgment section*** finds the depth of each block from that path search information. An effective block judgment section compares the depth of each block to a specified depth that is stored in a specified depth storage section, and judges which blocks are effective blocks. ***Thus,***

blocks that include nodes that exert influence on the simulation accuracy at the node that is the object of analysis are extracted from the circuit that is the object of simulation as effective blocks. Then, in the circuit simulation, events are generated only for the effective blocks, and a transient analysis simulation is executed by the event-driven method. This permits the processing speed of the simulation to be increased while maintaining accuracy. See fig. 3, 5-6, 14; col. 1, line 66 to col. 3, line 25.

Response to Arguments

28. Applicant's arguments filed 12/21/2000 have been fully considered but they are not persuasive.

29. The objection to the drawings has been withdrawn.

30. The Examiner has carefully considered Representative's arguments concerning the 101 rejections (pp. 5-6, paper # 12); the Representative is referred to the rejection, repeated above.

31. With respect to Representative's arguments concerning the 112 rejections (pp. 6-9, paper # 12) and the art rejections (pp. 9-13, paper # 12), the Examiner again notes that many of the argued features are *not actually claimed* (also, please the 112 rejections, above). For example, the matter disclosed on page 10 is simply not present in claim 45, for example.

32. With respect to Representative's arguments concerning the 112(1) rejections (pg. 6, paper # 12) the Examiner notes that the Representative has referred to examples. However, the issue as discussed in paragraph 8, paper # 6 has not been satisfactorily resolved.

33. Representative's arguments concerning the 112(2) rejections (pp. 6-9, paper # 12) are not deemed persuasive. In response to applicant's argument concerning the 112(2) rejections, it is noted that the features upon which applicant relies (i.e., *those at issue in the 112(2) rejections*) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). Applicant's invention must be clearly claimed. Please review the 112(2) rejections, repeated above.

34. Representative's arguments concerning the Filseth rejection (pp. 10-12, paper # 12), appear to be conclusary statements (regarding "*different technology*" or regarding claims of *faster simulation speeds*).

35. With respect to Representative's arguments concerning the Shinsha rejection (pp. 12-13, paper # 12), Shinsha discloses a logic design automation system examines correspondence relationship among sublogics in intermediate gate-level logic (containing neither physical design information nor manually optimized logic design information) produced from updated functional-level logic and current gate-level logic (containing the above information) to identify corresponding sublogics and non-corresponding sublogics of the gate-level logics with reference to primary input/output signals and input/output gates. ***For the corresponding sublogics, the corresponding sublogics of the current gate-level logic are selected, and for the non-corresponding sublogics, the non-corresponding sublogics of the intermediate gate-level logic are selected. The selected sublogics are combined to synthesize updated gate-level logic which***

preserved therein the physical design information and the manually optimized logic design information for portions of the current gate-level logic which need not be modified.

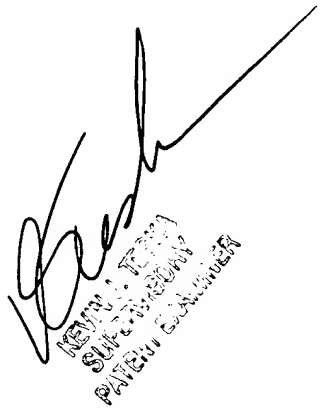
36. With respect to Representative's arguments concerning the Wang rejection (pg. 13, paper # 12), see pg. 261 (Wang).

37. With respect to Representative's arguments concerning the Kuehlmann rejection (pg. 13, paper # 12), see section 2 (Kuehlmann).

38. In response to applicant's arguments against the references individually (pp. 11-13, paper # 12), one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

39. Examiner would like to thank Representative for the description of one of the embodiments (page 10, paper # 4). This description indicates, to the Examiner, the possible existence of novel matter. However, as stated in paper # 6, this matter *still has not been claimed.*

40. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dr. Hugh Jones whose telephone number is (703) 305-0023.



Dr. Hugh Jones

January 10, 2001